Attorney Docket No. 10559-395001
Appl. No. 09/823,095
Amendment dated Oct ber 29, 2003
Reply to Office Action dated August 28, 2003

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Amendments to the Specification:

Please replace the paragraph beginning at page 6, line **OFFICIAL**

[0018] with the following amended paragraph:

By way of example, an instruction set supported by the
processor 2 may include instructions of varying widths. For
instance, instructions may be 16 bit instructions, 32 bit
instructions, or 64 bit instructions. The control unit 5 may
cause data blocks to be loaded into the 64 bit prefetch buffers.
An instruction may therefore reside in one of the prefetch
buffers 16, 17, or alternatively an instruction may be spread
across the prefetch buffers 16, 17. The control unit 5 may also
generate exception status information, for instance, describing
the exception status of the instructions contained in a given
data block. Thus, if an instruction is spread across the
prefetch buffers 16, 17 it may have exception status information
associated with both data blocks that contain part of the
instruction.

Please replace the paragraph beginning at page 7, line

[0019] with the following amended paragraph:

Because more than one instruction may be contained in a
given ~~the~~ prefetch buffer 16, 17, or a given instruction may be

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spread across the prefetch buffers 16, 17, the instruction

alignment unit 8 may ensure that an instruction is properly

aligned when the control unit 5 issues the instruction to

execution unit 4. The instruction alignment unit 8 may include

one or more alignment multiplexers 20 to ensure proper

instruction alignment. When an instruction is issued to

execution unit 4, at least part of the exception status

information associated with the instruction may be sent to the

exception management logic 9.

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